CLAIMS

1. A method of manufacturing an insulated gate field effect transistor; including:

providing a substrate (2) having a first major surface having a low-doped region (4) at the first major surface, the low-doped region having a concentration of less than $5x10^{14}$ cm^{-3} at the first major surface;

forming gate trenches (8) extending from the first major surface;

forming trench insulator (12,14) on the base and sidewalls of the gate trenches;

implanting dopants of a first conductivity type at the base of the trenches;

implanting a body implant of second conductivity type opposite to the first conductivity type in the low-doped regions between the trenches;

carrying out a diffusion step to form an insulated gate transistor structure in which the body implant diffuses towards the substrate (2) in the low doped region to form a p-n junction between a body region (22) doped to have the second conductivity type above a drain region (20) doped to have the first conductivity type, the p-n junction being deeper below the first major surface between the trenches than at the trenches; and

forming source regions (18) at the first major surface adjacent to the trench.

2. A method according to claim 1 in which the p-n junction boundary between drain and body is deeper between the trenches than the depth of the trenches.

3. A method according to claim 1 or 2 in which the structure formed in the diffusion step has an additionally doped region (26) of first conductivity type at the base of the gate trenches having a doping density below $5x10^{16}$ cm^{-3} but higher than in the drain regions (20) between the trenches.

4. A method according to claim 1, 2 or 3 wherein the step of implanting a body implant implants the body implant has a dose of at most $5x10^{13}$ cm^{-2}.

5. A method according to any preceding claim further comprising the step of forming a pattern laterally across the first major surface of the substrate, the pattern doped to have lower-doped regions (92) of first conductivity type alternating with higher-doped regions (90) of first conductivity type,

wherein the gate trenches (10) are formed in the higher-doped regions (90).

6. A method according to claim 5 wherein:

the step of forming a pattern laterally across the first major surface of the substrate includes:

depositing an epilayer (4) of semiconductor doped to have a lower doping density;

patterning a plurality of trench etch windows (8) spaced laterally across the substrate; and

implanting dopants (90) though the trench etch windows, the dopants being of a first conductivity type;

wherein the step of forming gate trenches (10) in the higher doped regions (90) includes etching gate trenches through the trench etch windows.

7. A method according to claim 5 wherein the step of forming a pattern laterally across the first major surface of the substrate includes:

etching a plurality of semiconductor trenches spaced laterally across the substrate in a layer of lower doping density;

and

growing semiconductor doped to have a higher doping density in the semiconductor trenches.

8. A method according to any preceding claim wherein the semiconductor (2) is silicon and the first conductivity type is n-type.

9. A method according to any preceding claim for making an insulating gate transistor of predetermined breakdown voltage for which the doping of a an epilayer (4) for forming a conventional insulated gate field effect transistor without the step of implanting dopant at the gate of the trench has a first predetermined doping concentration;

wherein the doping of the low doped region (4) at the first major surface is at most one half of the predetermined doping concentration.

10. A method according to any preceding claim, further comprising performing a moat etch by etching the semiconductor away from the trenches to a depth below the bottom of the source region.

11. A trench FET formed by a method according to any preceding claim.